

**3D Integrated eWLB /FO-WLP Technology
for PoP & SiP**

by

**Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and *Seung Wook Yoon
STATS ChipPAC Pte Ltd. 5 Yishun Street 23, Singapore 768442**

***STATS ChipPAC Pte Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059**

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STATS ChipPAC Pte Ltd 5 Yishun Street 23, Singapore 768442

*STATS ChipPAC Pte Ltd 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059

seungwook.yoon@statschppac.com

Abstract

Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand [4]

3D eWLB-PoP offers significant advantages in thin profiles and lower cost compared to current PoP technologies, particularly for mobile or tablet applications. 3D eWLB-PoP bottom has a 300um package height enabling a total stacked PoP height to be less than 0.8 mm after top

integration is also a growing trend for advanced application processors, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[6]

Figure 5 shows 3D eWLB^B SiP/module which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB^B-PoP to form a 3D SiP/ module with a thin package profile of total height of 1.0mm. 12 discretes of inductor and capacitors MLCC were removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. These discretes are also more power effective when they are close to the device, which significantly improves the overall electrical performance as well as provides a power saving advantage.

Functional test sample was prepared with power management integrated circuit (PMIC) as shown in Figures 5. It was a 6x6mm package size with a 4x4mm Si die and 12 discretes on top. This 3D eWLB^B SiP demonstrated more attractive power efficiency performance compared to other embedded package technology and it is representative of a significantly smaller packaging solution.

Figure 5. Photographs of 3D SiP eWLB-PoP with discretes on interposer or top package of discretes.

MEMS/Sensor eWLB

eWLB^B/FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, RF module, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[7]

Figure 6 shows eWLB^B sensor which has miniaturized from original side-by-side LGA package. It has 3D vertical

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